

NUP412VP5

Low Capacitance Quad Array for ESD Protection

This integrated transient voltage suppressor device (TVS) is designed for applications requiring transient overvoltage protection. It is intended to be used in sensitive equipment such as wireless headsets, PDAs, digital cameras, computers, printers, communication systems, and other applications. The integrated design provides very effective and reliable protection for four separate lines using only one package. This device is ideal for situations where board space is at a premium.

Features

- ESD Protection: IEC61000-4-2: Level 4
- Four Separate Unidirectional Configurations for Protection
- Low Leakage Current < 1 μ A @ 9 V
- Small SOT-953 SMT Package
- Low Capacitance
- These are Pb-Free Devices

Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Protects Four Lines Against Transient Voltage Conditions
- Minimize Power Consumption of the System
- Minimize PCB Board Space

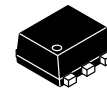
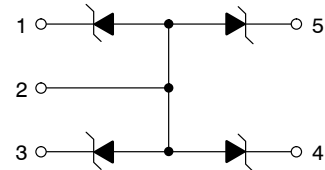
Typical Applications

- Cellular and Portable Electronics
- Serial and Parallel Ports
- Microprocessor Based Equipment
- Notebooks, Desktops, Servers



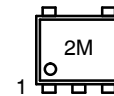
ON Semiconductor®

<http://onsemi.com>



**SOT-953
CASE 526AB**

MARKING DIAGRAM



2 = Specific Device Code
M = Date & Assembly Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|----------------------|-----------------------|
| NUP412VP5T5G | SOT-953 (Pb-Free) | 8000 / Tape & Reel |

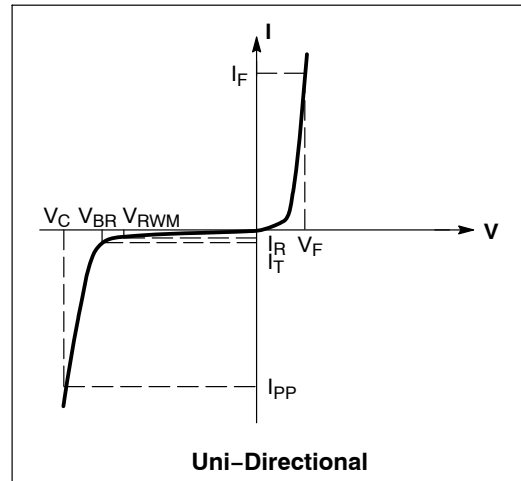
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP412VP5

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| ΘV_{BR} | Maximum Temperature Coefficient of V_{BR} |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| Z_{ZT} | Maximum Zener Impedance @ I_{ZT} |
| I_{ZK} | Reverse Current |
| Z_{ZK} | Maximum Zener Impedance @ I_{ZK} |



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Value | Unit |
|--|-----------------|-------------|--|
| Peak Power Dissipation (8 X 20 μs @ $T_A = 25^\circ\text{C}$) (Note 1) | P_{PK} | 18 | W |
| Thermal Resistance Junction-to-Ambient Above 25°C , Derate | $R_{\theta JA}$ | 560 4.5 | $^\circ\text{C/W}$ $\text{mW}/^\circ\text{C}$ |
| Maximum Junction Temperature | T_{Jmax} | 150 | $^\circ\text{C}$ |
| Operating Junction and Storage Temperature Range | $T_J T_{stg}$ | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature (10 seconds duration) | T_L | 260 | $^\circ\text{C}$ |
| Human Body Model (HBM) Machine Model (MM) | ESD | 8000 400 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Non-repetitive current.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

| Device | Device Marking | Breakdown Voltage V_{BR} @ 5 mA (Volts) | | | Leakage Current I_{RM} @ V_{RM} | | Typ Capacitance @ 0 V Bias (pF) (Note 2) | | Typ Capacitance @ 3 V Bias (pF) (Note 2) | |
|--------------------|----------------|---|-----|------|-------------------------------------|-----------------------------|--|-----|--|-----|
| | | Min | Nom | Max | V_{RWM} | I_{RWM} (μA) | Typ | Max | Typ | Max |
| NUP412VP5 (Note 3) | 2 | 11.4 | 12 | 12.7 | 9.0 | 0.5 | 6.5 | 10 | 3.5 | 5.0 |

2. Capacitance of one diode at $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$.

3. V_{BR} at 5 mA.

NUP412VP5

TYPICAL ELECTRICAL CHARACTERISTICS

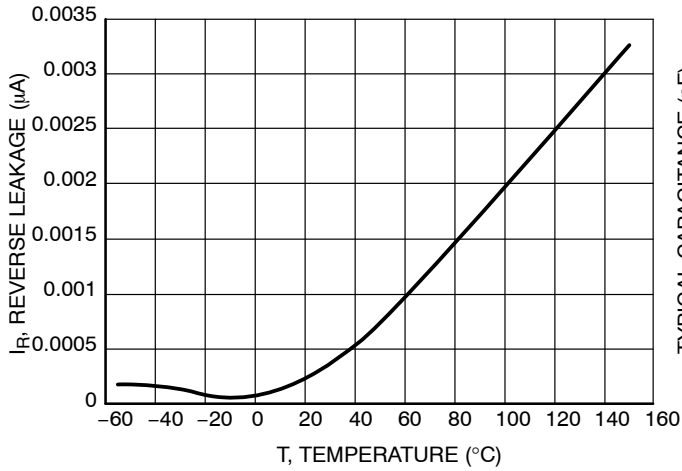


Figure 1. Reverse Leakage versus Temperature

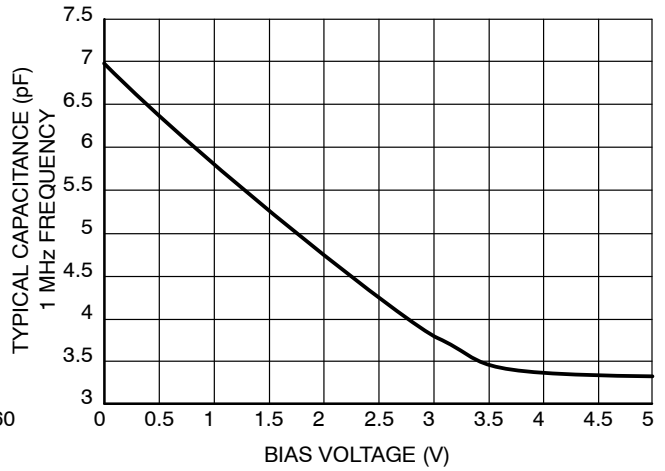


Figure 2. Capacitance

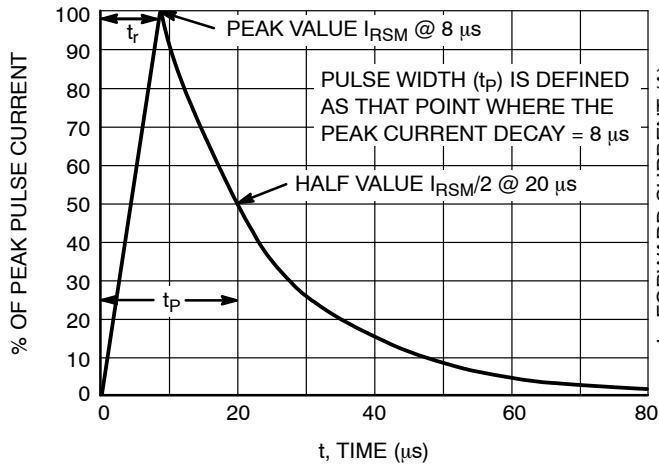


Figure 3. 8 × 20 μs Pulse Waveform

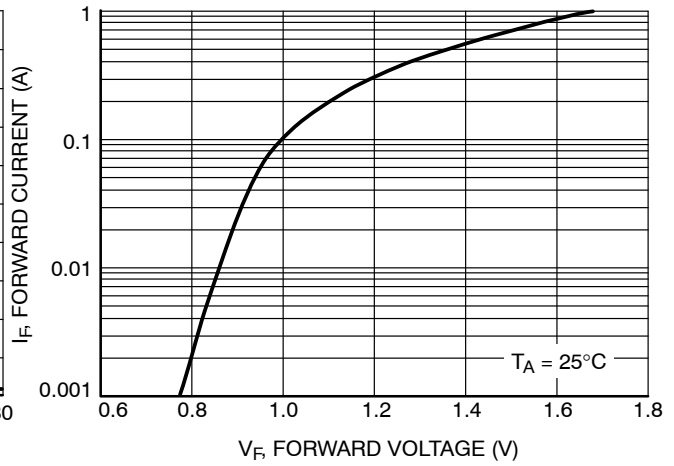


Figure 4. Forward Voltage

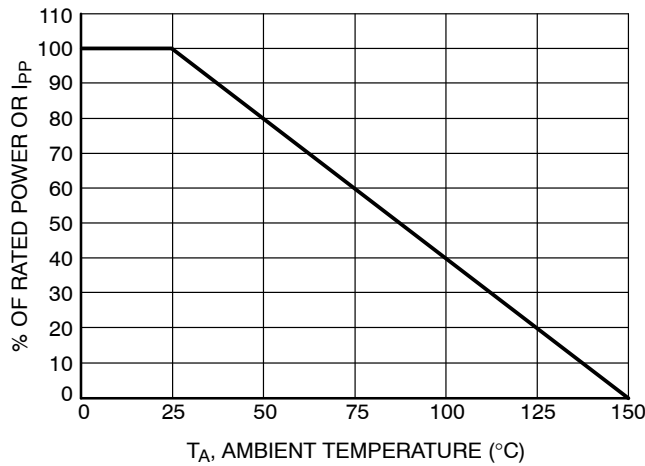
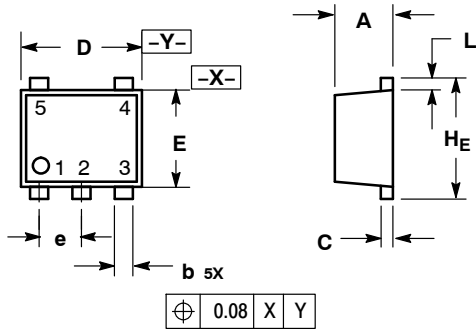


Figure 5. Power Derating Curve

NUP412VP5

PACKAGE DIMENSIONS

SOT-953
CASE 527AB-01
ISSUE B

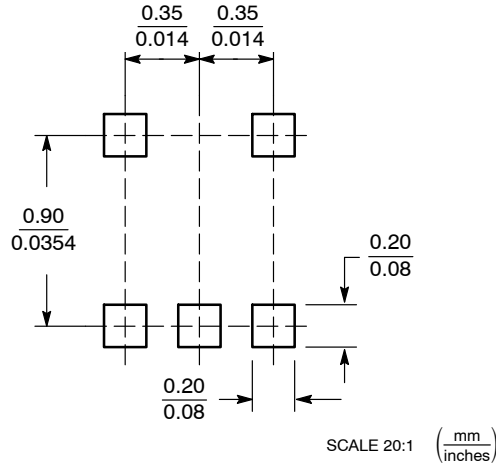


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.34 | 0.42 | 0.50 | 0.013 | 0.017 | 0.020 |
| b | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| C | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| D | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| E | 0.75 | 0.80 | 0.85 | 0.03 | 0.032 | 0.034 |
| e | 0.35 BSC | | | 0.014 BSC | | |
| L | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| HE | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative